

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Gheorghe C. Cascaval, et al.

Examiner: Unassigned

Serial No: To Be Assigned

Art Unit: Unassigned

Filed: Herewith

Docket: YOR920030301US1 (16832)

**For: A MECHANISM FOR ON-LINE
PREDICTION OF FUTURE
PERFORMANCE MEASUREMENTS
IN A COMPUTER SYSTEM**

Dated: October 17, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.


1. Allan Snavely, et al. "Symbolic Jobscheduling with Priorities for a Simultaneous Multithreading Processor", *International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS)*, June 2002;
2. Sujay Parekh, et al. "Thread-Sensitive Scheduling for SMT Processors", *University of Washington Technical Report*, Pages 1-18; 2000; and

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I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box Alexandria, VA 22313-1450 on October 17, 2003.

Dated: October 17, 2003

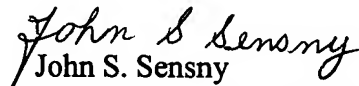

Steven Fischman

3. Christos D. Antonopoulos, et al. "Scheduling Algorithms with Bus Bandwidth Consideration for SMP's", *International Conference on Parallel Processing*, Pages 1-21; Tawain, October 2003.

Applicants are submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,


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